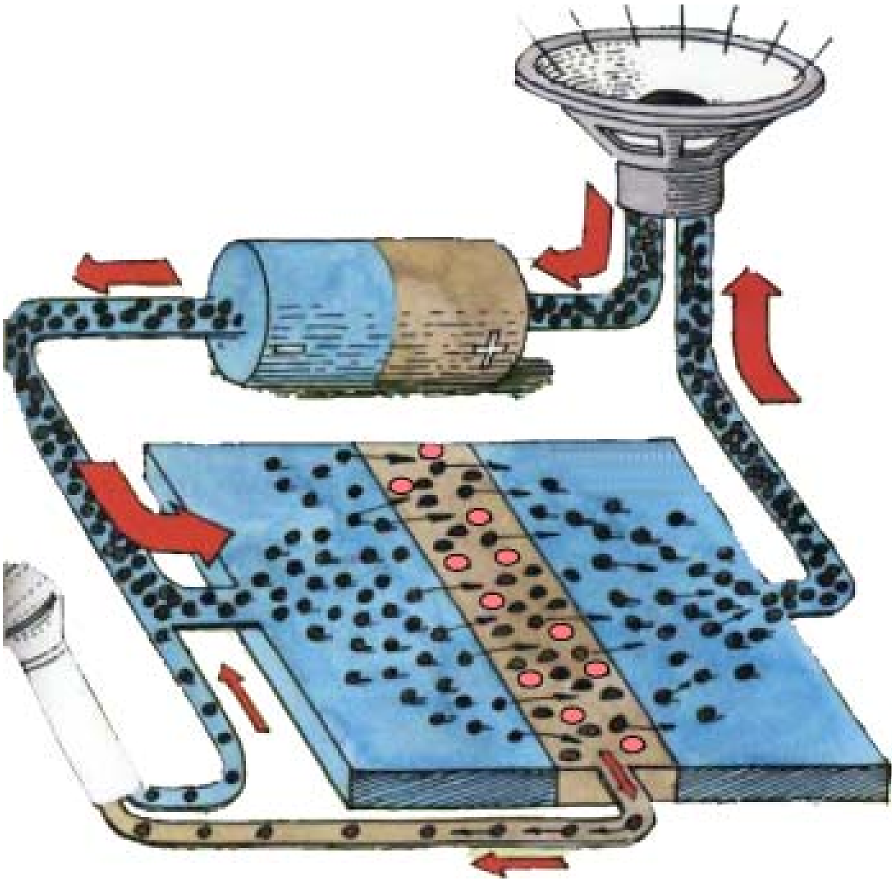
Analogue Coursework — Part 1

Design of a JFET/BJT common-drain / common-emitter cascade amplifier with an approximate 3dB low-frequency cut-off of 50Hz.



UNIVERSITY of ULSTER — school of electrical and mechanical engineering

COURSE: BEng (HONS) Electronic Systems
MODULE: EEE508J1 - Electronic Circuit Design
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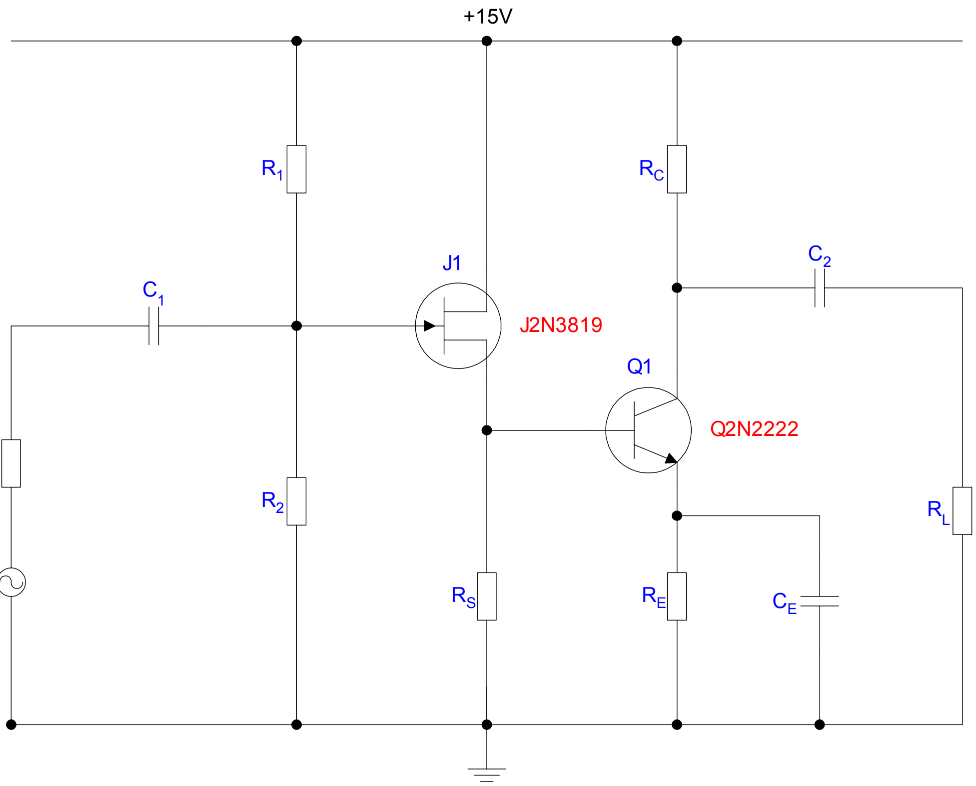
DATE: 10/11/2001

CONTENTS

(a) Design a JFET/BJT common-drain / common-emitter cascade amplifier

Using a 15V power supply, with an approximate 3dB low-frequency cut-off of 50Hz. The amplifier input is capacitive coupled to a 10KΩ source and the output is capacitive coupled to a 1kΩ load. Transistors J2N3819 and Q2N2222 are available in the circuit simulation package PSpice.

Circuit diagram shown below (resistor and capacitor values will be calculated): -



Available transistors have the following parameter values (from datasheets): -

J2N3819
I_{DSS} = 10mA
$|V_p|$ = 3V

Q2N2222
V_A = 74V
$h_{fe} = \beta = 150$

Note: V_{CC} = 15V
RL = 1KΩ
R = 10KΩ
3dB low-frequency cut-off of 50Hz

Resistor design by inspection

Let $$I_D = \frac{I_{DSS}}{4} = \frac{10\times10^{-3}}{4} = 2.5\text{mA}$$

$$V_{GS} = \frac{V_p}{2} = \frac{-3}{2} = -1.5\text{V}$$

Let $I_C = 1\text{mA}$

Let $V_G = \frac{V_{CC}}{3} = \frac{15}{3} = 5\text{V}$

Let R_2 = 500K => $R1$ = 1MΩ

$V_S = V_G + |V_{GS}| = 5 + 1.5 = 6.5\text{V}$

$$R_S = \frac{V_S}{I_D} = \frac{6.5}{2.5 \times 10^{-3}} = 2.6 \times 10^3 = 2.6\text{K}\Omega$$

$V_E = V_S - 0.7 = 6.5 - 0.7 = 5.8\text{V}$

$$R_E = \frac{V_E}{I_C} = \frac{5.8}{1 \times 10^{-3}} = 5.8 \times 10^3 = 5.8\text{K}\Omega$$

Let $V_C = \frac{2V_{CC}}{3} = 10\text{V}$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{15 - 10}{1mA} = 5\text{K}\Omega$$

Capacitor design using method of short-circuit timer constants

f = 50Hz

Using the method of short-circuit time constants, the low-frequency cut-off ω_L is given by

$$1.15\varpi_L \approx \sum_{i=1}^{N} \frac{1}{C_i R_{is}} = \frac{3}{\tau}$$

Since this expression is generally accurate, whether or not a dominant pole exists, it is convenient to make the entire time-constants equal, so that each capacitor plays and equal role in determining the 3dB cut-off frequency. Let the time-constant be donated by τ .

$$\varpi_L = 2\pi f = 2\pi 50 = 100\pi \qquad \tau = \frac{3}{1.15 \times 100\pi} = 8.30374 \times 10^{-3}$$

Design of C_1

C_1 “sees” resistance R and R_{in}.

$$R_{in} = R_1 \ || \ R_2 = \frac{500\text{K} \times 1\text{M}}{500\text{K} + 1\text{M}} = \frac{500 \times 10^9}{1.5 \times 10^6} = 333.33\text{K}\Omega$$

$$C_1 = \frac{\tau}{R + R_{in}} = \frac{8.3 \times 10^{-3}}{10\text{K} + 333\text{K}} = 24.1983 \times 10^{-9} = 24.2\text{nF}$$

Design of C_2

C_2 "sees" resistance R_O and R_L.

$R_O = R_C \,||\, r_O$

$$r_O = \frac{V_A}{I_C} = \frac{74}{1 \times 10^{-3}} = 74\text{K}\Omega$$

$$R_O = 5\text{K} \,||\, 74\text{K} = \frac{5\text{K} \times 74\text{K}}{5\text{K} + 74\text{K}} = \frac{370 \times 10^6}{79 \times 10^3} = 4.68354 \times 10^3 = 4.68\text{K}\Omega$$

$$C_2 = \frac{\tau}{R_O + R_L} = \frac{8.3 \times 10^{-3}}{4.68\text{K} + 1\text{K}} = \frac{8.3 \times 10^{-3}}{5.68 \times 10^3} = 1.46127 \times 10^{-6} = 1.46\mu\text{F}$$

Design of C_E

C_E "sees" resistance $R_E \,||\, \left\{ r_e + \frac{R_{oi}}{\beta} \right\}$.

$$R_{oi} = R_S \,||\, \frac{1}{g_m}$$

$$g_m = \frac{2I_{DSS}}{|V_p|}\sqrt{\frac{I_D}{I_{DSS}}} = \frac{2 \times 10 \times 10^{-3}}{3}\sqrt{\frac{2.5 \times 10^{-3}}{10 \times 10^{-3}}} = 3.3333 \times 10^{-3} = 3.333\text{mA/V}$$

$$R_{oi} = 2.6\text{K} \,||\, \frac{1}{3.3333 \times 10^{-3}} = \frac{2.6\text{K} \times 300}{2.6\text{K} + 300} = \frac{780 \times 10^3}{2.9 \times 10^3} = 268.966 = 268.97\Omega$$

$$r_e = \frac{25\text{mV}}{\text{I}_\text{E}} = \frac{25 \times 10^{-3}}{1 \times 10^{-3}} = 25\Omega$$

$$R_E \,||\, \left\{ r_e + \frac{R_{oi}}{\beta} \right\} = 5.8\text{K} \,||\, \left\{ 25 + \frac{268.97}{150} \right\} = 5.8\text{K} \,||\, 26.79 = \frac{5.8\text{K} \times 26.79}{5.8\text{K} + 26.79} = 26.6699\Omega$$

$$C_E = \frac{\tau}{33.802} = \frac{8.3 \times 10^{-3}}{26.6699} = 311.212 \times 10^{-6} = 311.21\mu F$$

(b) Estimate the input resistance, the output resistance and the voltage gain

$$R_{in2} = \beta r_e = 150 \times 25 = 3.75\text{K}\Omega$$

$$\frac{V_S}{V_g} = \frac{R_S \,||\, R_{in2}}{\{R_S \,||\, R_{in2}\} + \frac{1}{g_m}} = \frac{2.6\text{K} \,||\, 3.75\text{K}}{\{2.6\text{K} \,||\, 3.75\text{K}\} + 300} = \frac{1.53543 \times 10^3}{1.83543 \times 10^3} = 0.836551$$

$$\frac{V_g}{V} = \frac{R_{in}}{R_S + R_{in}} = \frac{333.33 \times 10^3}{2.6 \times 10^3 + 333.33 \times 10^3} = \frac{333.33}{335.93} = 0.99226$$

$$\frac{V_O}{V_S} = \frac{R_C \,||\, R_L \,||\, r_O}{r_e} = \frac{5\text{K} \,||\, 1\text{K} \,||\, 74\text{K}}{25} = \frac{824.053}{25} = 32.9621 = 33$$

$$\frac{V_O}{V} = \frac{V_S}{Vg} \times \frac{V_g}{V} \times \frac{V_O}{V_S} = 0.836551 \times 0.99226 \times 32.9621 = 27.3611$$

Voltage gain = $\frac{V_O}{V}$ = 27.36

Input resistance (R_{in}) was calculated during the design of C_1: -

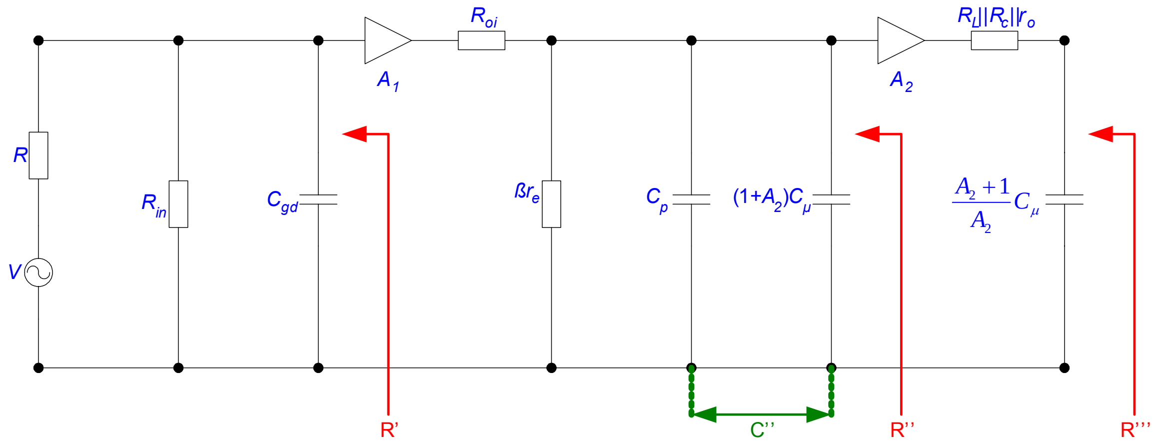
R_{in} = 333.33KΩ

Output resistance (R_O) was calculated during the design of C_2: -

R_O = 4.68 KΩ

(c) Draw a high-frequency equivalent circuit and estimate 3_{dB} high-frequency cut-off

Neglecting r_X and C_{gs}, high frequency equivalent for the cascade amplifier circuit is: -



Transistors have the following parameter values (from PSpice output file): -

J2N3819
C_{gd} = 671 x 10^{-15} = 0.671pF
g_m = 3.68 x 10^{-3}

Q2N2222
C_μ = 4.11 x 10^{-12} = 4.11pF
C_π = 52.5 x 10^{-12} = 52.5pF
F_T = 111 x 10^6 = 111MHz
r_X = 10Ω
r_O = 75.6 x 10^3 = 75.6kΩ

We have all the values contained within the equation: -

$$f_T = \frac{1}{2\pi r_e\left(C_\mu + C_\pi\right)}$$

Let's test this equation, put values C_μ, C_π and r_e into equation and compare calculated f_T with the value of f_T contained in the PSpice output file.

$$f_{T_{CAL}} = \frac{1}{2\pi 25\left(4.11\times10^{-12} + 52.5\times10^{-12}\right)} = \frac{1}{8.89228\times10^{-9}} = 112.457\times10^6 = 112.5\text{MHz}$$

It's clear that the equation above for working out f_T offers an extremely good approximation, as there was only difference of 1.313% between the calculated value and the PSpice value.

Calculation of f_{n1}

$$R' = R_{in} \,||\, R = 333.33\text{K} \,||\, 10\text{K} = \frac{333.33\times10^3\times10\times10^3}{333.33\times10^3 + 10\times10^3} = \frac{3.3333\times10^9}{343.33\times10^3} = 9.70874\times10^3 = 9.709\text{K}\Omega$$

$$f_{n1} = \frac{1}{2\pi R' C_{gd}} = \frac{1}{2\pi 9.709\times10^3\times671\times10^{-15}} = \frac{1}{40.9322\times10^{-9}} = 24.4306\times10^6 = 24.43\text{MHz}$$

Calculation of f_{n2}

$$R_{oi} = R_S \,||\, \frac{1}{g_m} = 2.6\text{K} \,||\, \frac{1}{3.68 \times 10^{-3}} = 2.6\text{K} \,||\, 271.739 = 246.026 = 246\Omega$$

$$R'' = R_{oi} \,||\, \beta r_e = 246.026 \,||\, 3750 = \frac{246.026 \times 3750}{246.026 + 3750} = 230.879\Omega$$

A_2 = 32.96

$$C'' = C_\pi \,||\, (1 + A_2)C_\mu = C_\pi + \left((1 + A_2)C_\mu\right) = 52.5 \times 10^{-12} + \left((1 + 32.96)4.11 \times 10^{-12}\right) = 192.076 \times 10^{-12}$$

$$f_{n2} = \frac{1}{2\pi R'' C''} = \frac{1}{2\pi 230.879 \times 192.076 \times 10^{-12}} = \frac{1}{278.634 \times 10^{-9}} = 3.58891 \times 10^{6} = 3.6\text{MHz}$$

Calculation of f_{n3}

$$R''' = R_L \,||\, R_C \,||\, r_O = 1\text{K} \,||\, 5\text{K} \,||\, 75.6\text{K} = \frac{1}{\frac{1}{1 \times 10^3} + \frac{1}{5 \times 10^3} + \frac{1}{75.6 \times 10^3}} = 824.248\Omega$$

$$f_{n3} = \frac{1}{2\pi R''' \frac{A_2+1}{A_2} C_\mu} = \frac{1}{2\pi \times 824.248 \times \frac{33.96}{32.96} \times 4.11 \times 10^{-12}} = \frac{1}{21.9311 \times 10^{-9}} = 45.5974 \times 10^{6} = 45.6\text{MHz}$$

Calculation of 3_{dB} high-frequency cut-off (f_n)

Clearly a dominant pole exists at f_{n2} and we can write: -

$$f_n \approx 3.6\text{Mhz}$$

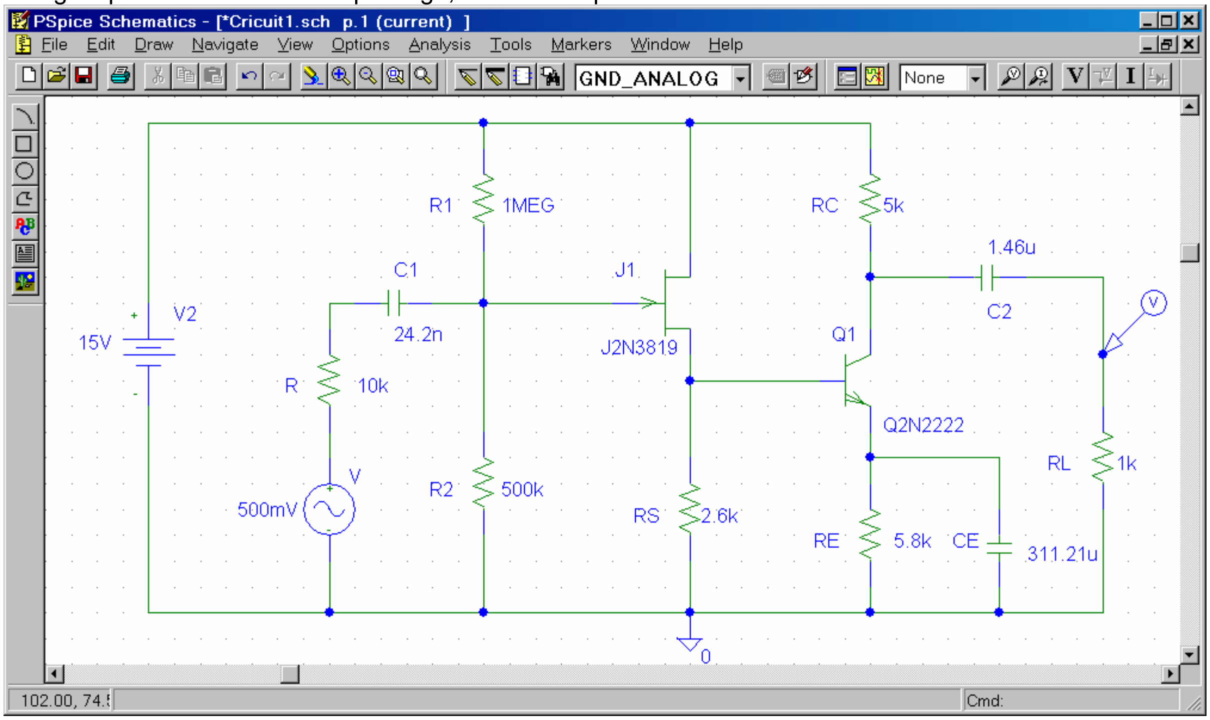
$$\frac{1.15}{f_n} = \frac{1}{f_{n1}} + \frac{1}{f_{n2}} + \frac{1}{f_{n3}}$$

$$\frac{1.15}{f_n} = \frac{1}{24.4\text{M}} + \frac{1}{3.6\text{M}} + \frac{1}{45.6\text{M}}$$

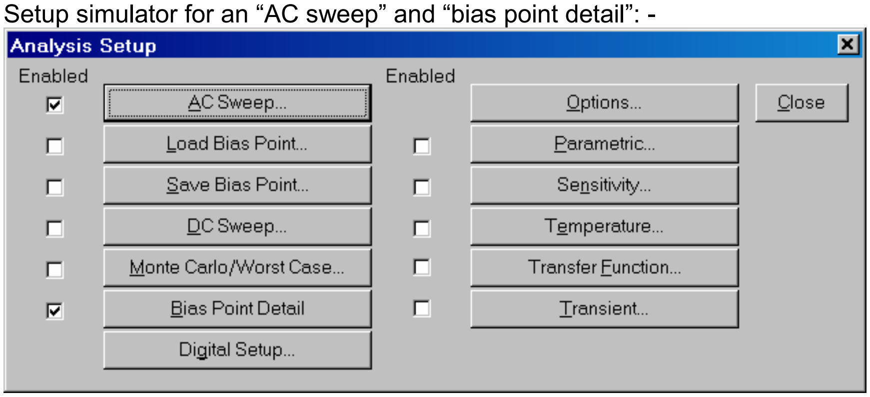
$$f_n = \frac{1.15}{\frac{1}{24.4\text{M}} + \frac{1}{3.6\text{M}} + \frac{1}{45.6\text{M}}} = \frac{1.15}{340.691 \times 10^{-9}} = 3.37549 \times 10^{6} = 3.4\text{MHz}$$

(d) Simulation of circuit and comparison of results with calculated / designed values

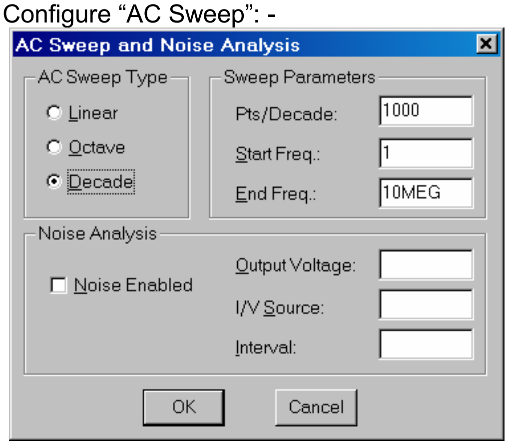
Using PSpice circuit simulation package, screen dump of circuit shown below: -



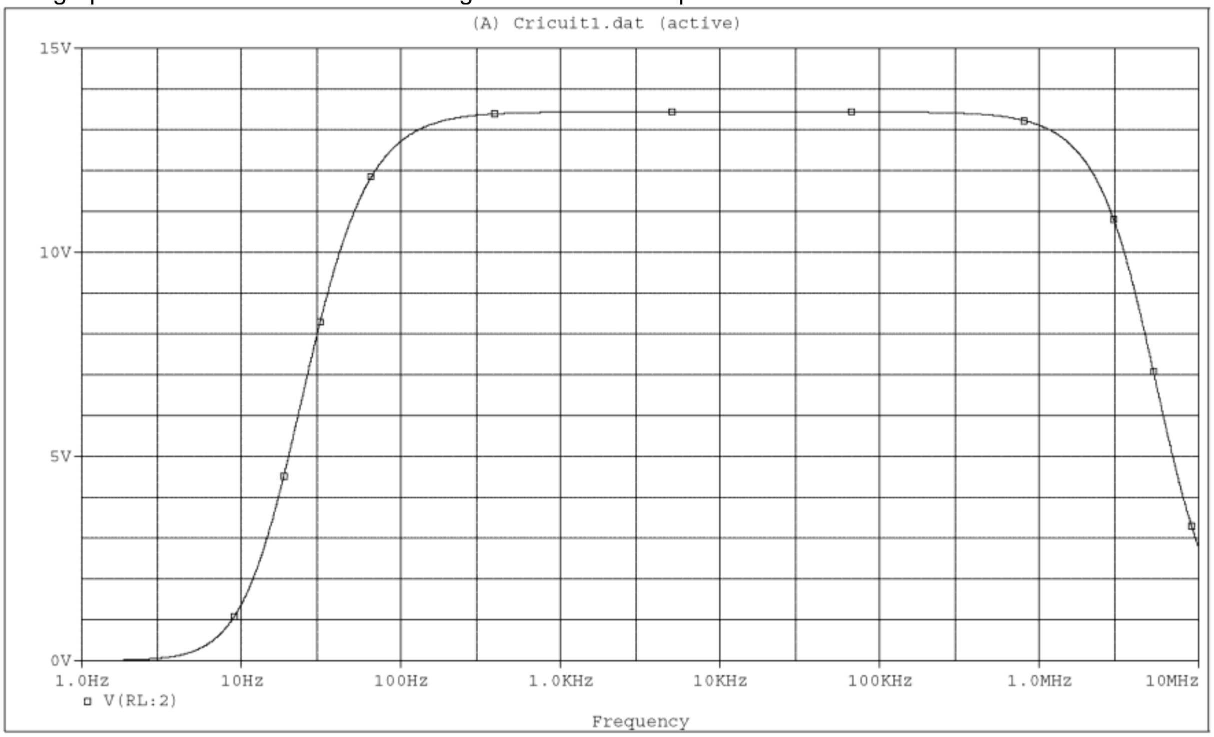
Setup simulator for an “AC sweep” and “bias point detail”: -



Configure “AC Sweep”: -



The graph below is the result of simulating the circuit under specified conditions: -



$$\text{Voltage Gain} = \frac{V_{MAX}}{V} = \frac{13.44}{.5} = 26.88$$

$$\text{Voltage Gain (dB)} = 20\log(26.88) = 28.5886\text{dB}$$

$$3_{\text{dB}}\ \text{Voltage Gain (dB)} = \text{Voltage Gain (dB)}\ -\ 3\ =\ 28.5886 - 3 = 25.5886\text{dB}$$

$$3_{\text{dB}}\ \text{Voltage Gain} = 10^{\frac{25.5886}{20}} = 19.0296$$

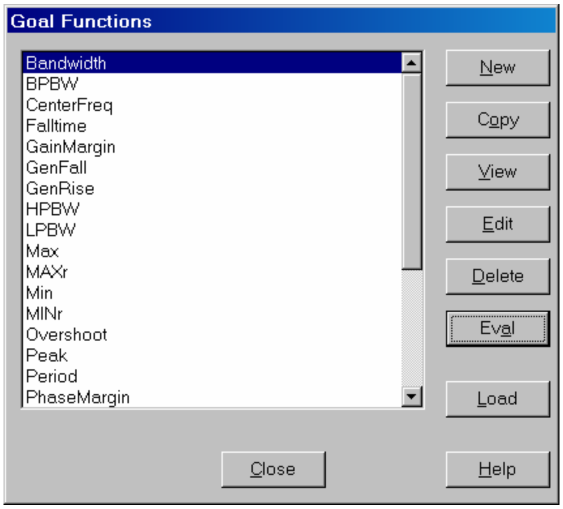
$$\text{3dB Voltage} = 3_{\text{dB}}\ \text{Voltage Gain} \times V = 19.0296 \times .5 = 9.51479\text{V}$$

Using “Probe Cursor”, get “low frequency cut-off”, “high frequency cut-off” and “Bandwidth”: -

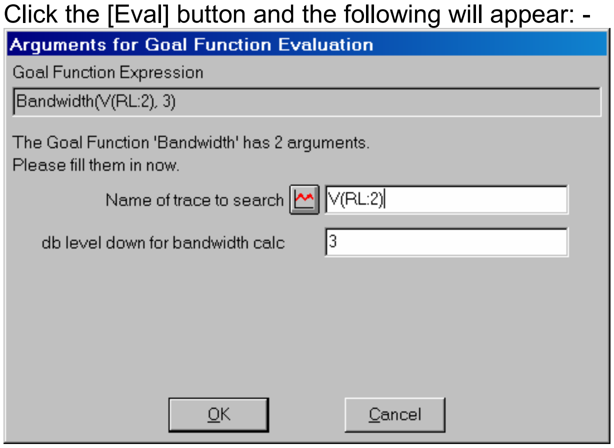
Probe Cursor		
A1 =	38.009,	9.527
A2 =	3.7078M,	9.515
dif=	-3.7078M,	12.085m

Low frequency cut-off $\approx$ 38.009Hz
High frequency cut-off $\approx$ 3.7078MHz
Bandwidth $\approx$ 3.7078MHz

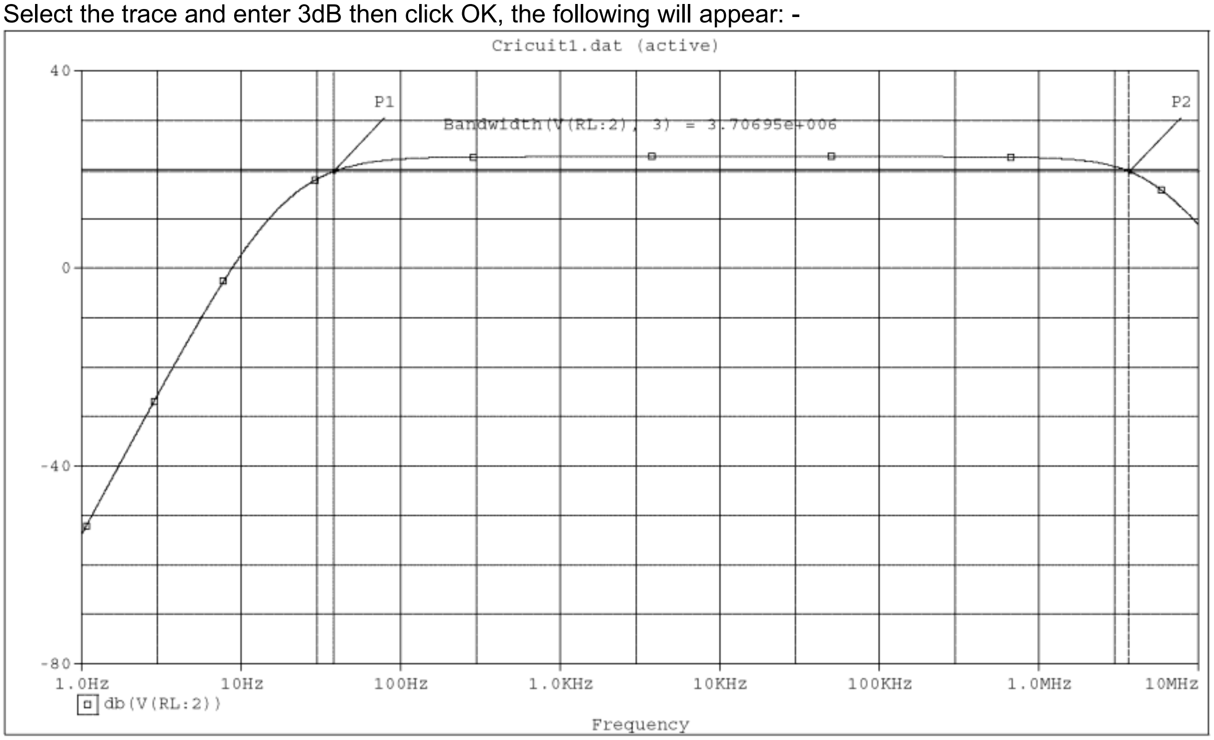
This is not the only way of getting “Low frequency cut-off”, “high frequency cut-off” and “Bandwidth using PSpice. A simpler way is to used the “Goal Functions” feature of PSpice, e.g. bring up the “Goal Functions” dialogue box from Menu item [Trace] [Goal Functions] and select the “Bandwidth” goal function. Screen dump of dialogue box shown below: -



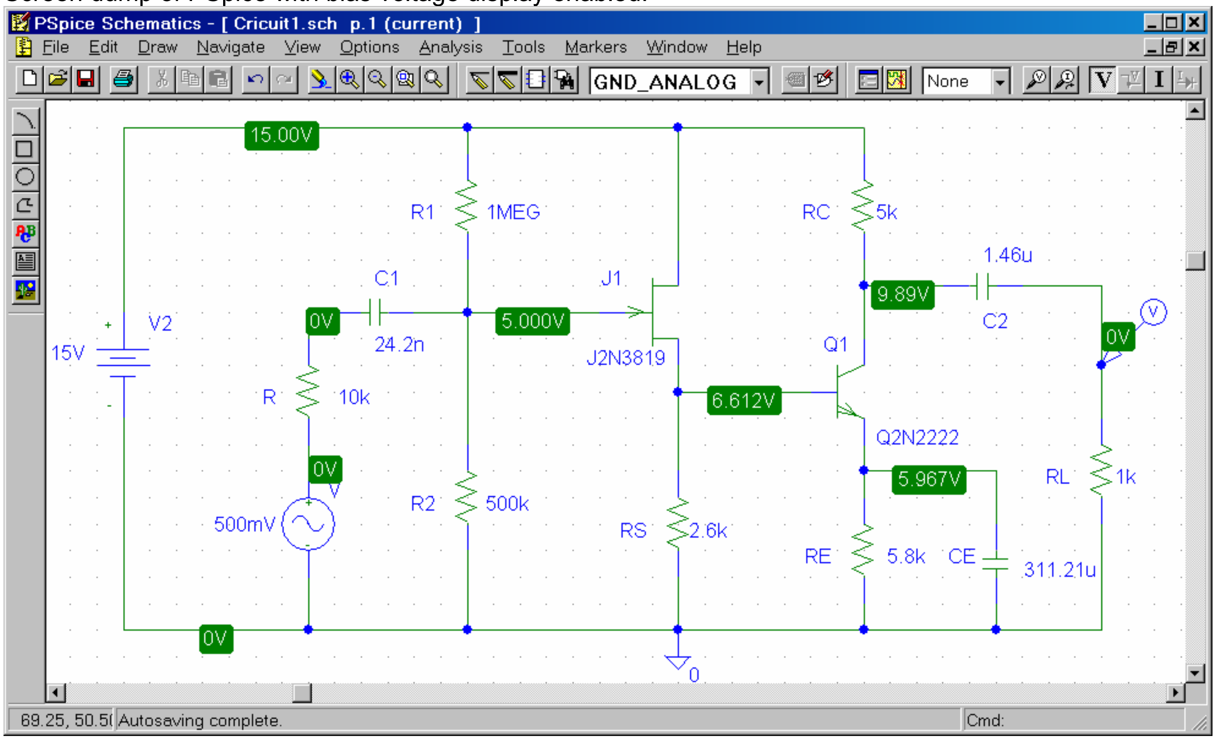
Click the [Eval] button and the following will appear: -



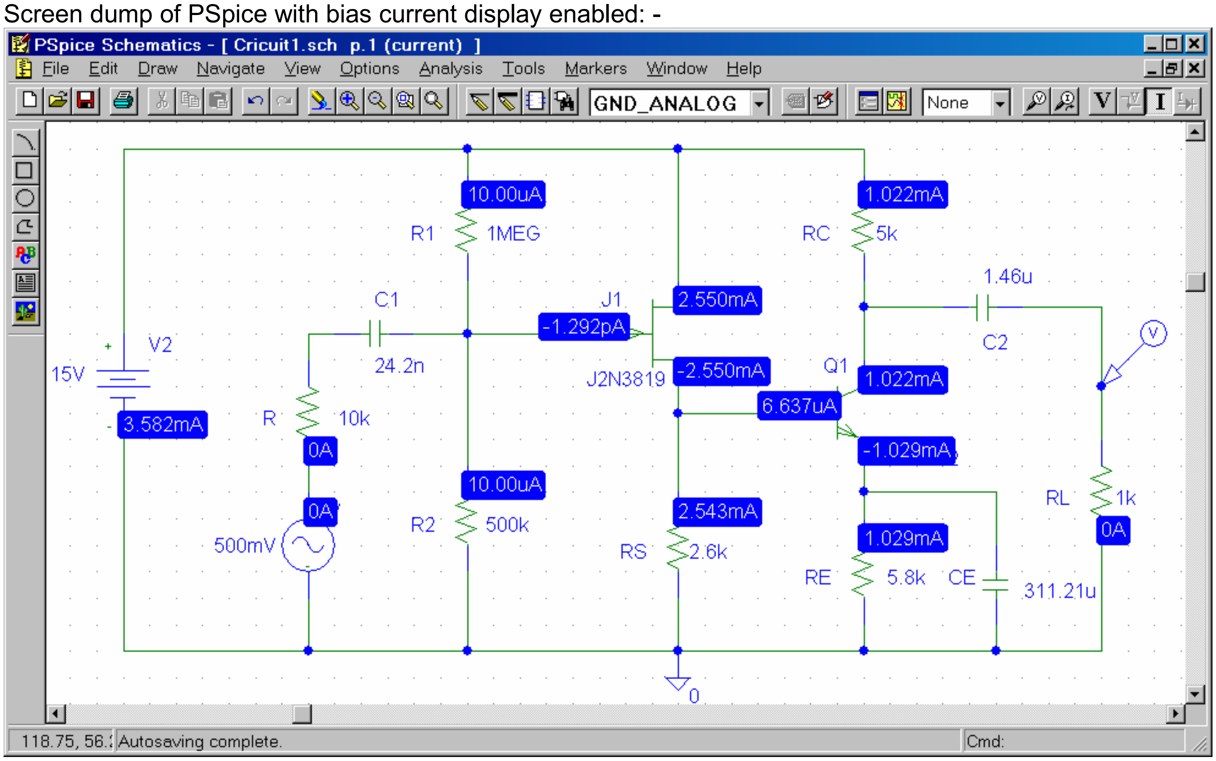
Select the trace and enter 3dB then click OK, the following will appear: -



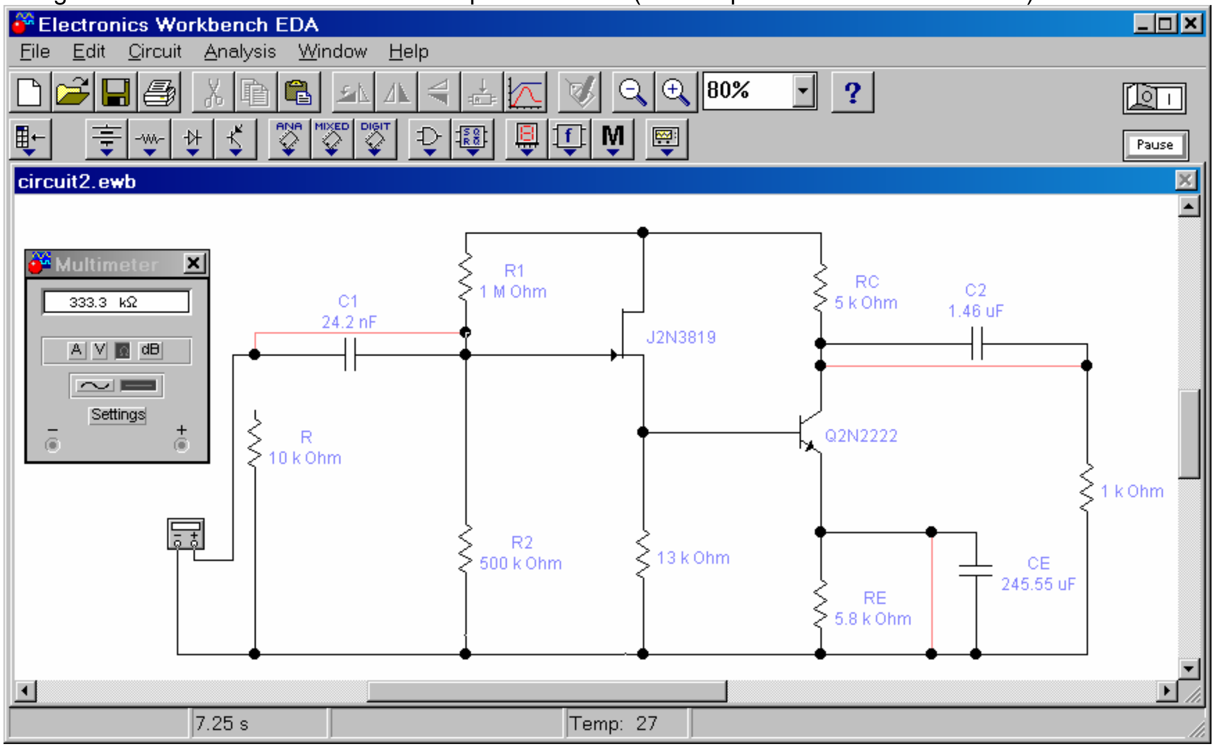
Screen dump of PSpice with bias voltage display enabled: -



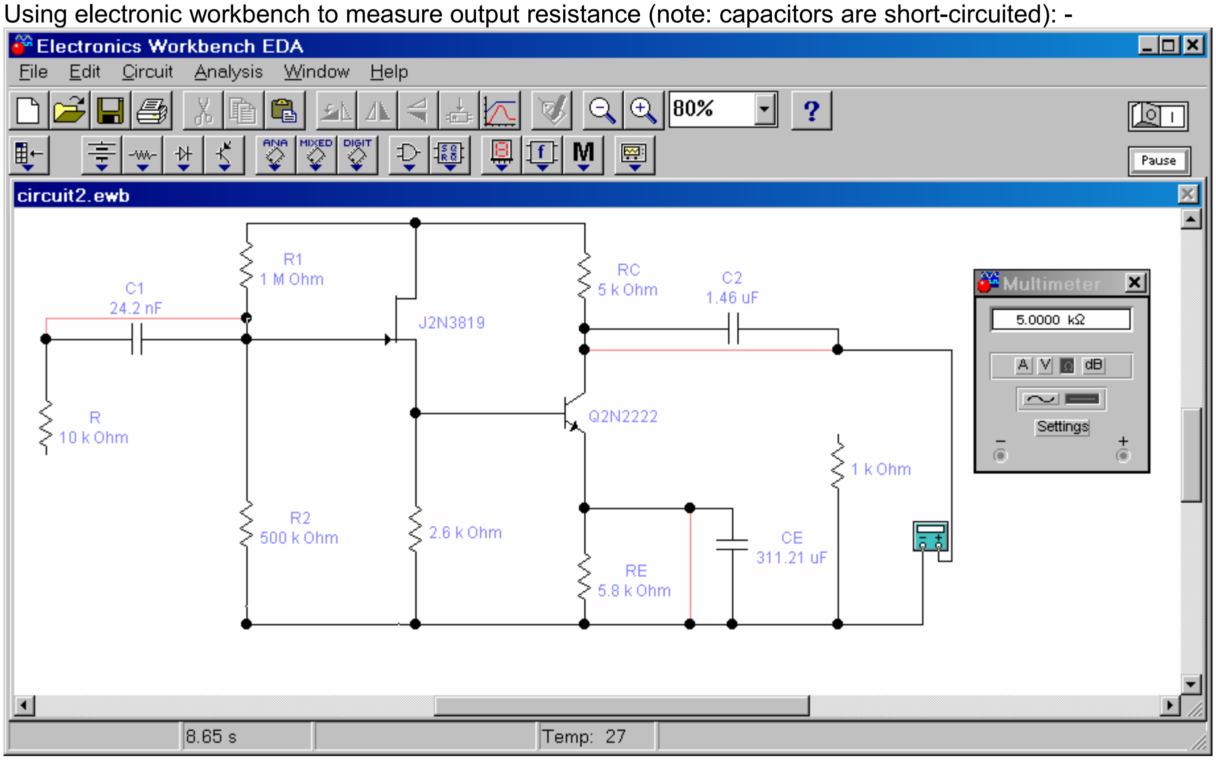
Screen dump of PSpice with bias current display enabled: -



Using electronic workbench to measure input resistance (note: capacitors are short-circuited): -



Using electronic workbench to measure output resistance (note: capacitors are short-circuited): -



Comparison Table

	Design / Calculated Value	Simulated Value	Difference	% Difference
I_D	2.5mA	2.55mA	0.05mA	2.00%
I_C	1mA	1.022mA	0.022mA	2.20%
I_S	2.5mA	2.543mA	0.043mA	1.72%
I_E	1mA	1.029mA	0.029mA	2.90%
V_G	5V	5V	0.00V	0.00%
V_{GS}	-1.5V	-1.61V	0.11V	7.33%
V_S	6.5V	6.612V	0.112V	1.72%
V_E	5.8V	5.967V	0.167V	2.88%
V_C	10V	9.89V	0.11V	1.11%
g_m	3.33mA/V	3.68mA/V	0.350mA/V	10.51%
r_o	74kΩ	75.6kΩ	1.6κΩ	2.15%
R_{in}	333.33KΩ	333.3kΩ	0.00kΩ	0.00%
R_O	4.68kΩ	5kΩ	0.32kΩ	6.84%
f_T	112.457MHz	111MHz	1.457MHz	1.31%
Low Frequency Cut-off	50Hz	38.01Hz	11.99Hz	31.54%
High Frequency Cut-off	3.4MHz	3.708MHz	0.308MHz	9.06%
Voltage Gain	27.36	26.88	0.48	1.79%

Conclusions

Simulated voltages (V_G,V_S, V_E, V_C) and currents (I_D, I_C, I_S, I_E) were extremely close (<3%) to the designed / calculated values. Proving the methods used in the design of the resistors are reasonable actuate. V_{GS} was 7.33% out, hence it's clear that the value of $|V_p|$ (from datasheet) used in the design of the amplifier was not 100% actuate as: -

$$V_{GS} = \frac{V_P}{2}$$

It is known that V_{GS} is -1.61V (from PSpice output file) hence V_P actually was -3.22V. If this value was used in the design of the amplifier it's would have produced more actuate results.

Notice g_m is 10.51% out, using the equation below it's clear that the value of I_{DSS} (from datasheet) used in the design of the amplifier may not be 100% actuate.

$$g_m = \frac{2I_{DSS}}{|V_p|}\sqrt{\frac{I_D}{I_{DSS}}}$$

Using PSpice values of g_m, V_p and I_D it is possible to calculate the actual value of I_{DSS}: -

$$I_{DSS} = \frac{{g_m}^2|V_P|^2}{4I_D} = \frac{\left(3.68\times10^{-3}\right)^2\times3.22^2}{4\times2.55\times10^{-3}} = 13.766\times10^{-3} = 13.77\text{mA}$$

If this correct value of I_{DSS} was used in the design of the amplifier it would have produce more actuate results.

The calculated voltage gain only differed by 1.79% with respect to the simulated PSpice value. Proving the technique used to calculated this voltage gain offers a reasonably actuate result.

The low frequency cut-off was a full 31.54% out, which tells us that something maybe wrong with the design. Although the low frequency cut-off was designed to be 50Hz or less, hence the objective has been achieved.

If the correct values of I_{DSS}, V_P and β were used in the design of the amplifier it may significantly improve the low frequency cut-off. Also the method used to calculate τ is an approximation and is not exact, and will have contributed to the error.

Percentage errors up to 10% are usually considered acceptable for analogue amplifier design. The high frequency cut-off differed by 9.06%, this error is acceptable and expected as the technique used in the calculation of high frequency cut-off is an approximation and is not exact.

Other reasons why design / calculated values differed from the simulated values: -

- Simulation packages like PSpice and electronic workbench simulate real life conditions including the tolerances of components: resistors (typically 1-2%), capacitors (typically 10-20%) and transistors etc…

- The operating temperature is simulated which affects the operation of the circuit. All simulations which were carried out on the amplifier were simulated with an operating temperature of 27^{o}C.

- Many of the formula used in the design are ROT (Rules of Thumb) which are designed for ease of use and may not be completely actuate.

It is possible to improve the design of an amplifier using a simulation package like PSpice, without making any calculations. For example capacitor values can be changed then simulate the output and make a note on how the low frequency cut-off is changed, using this method of trial-and-error it was discovered that if C_1 was changed to 14.2nF (instead of 24.2nF) the low frequency cut-off was be changed to 48Hz (improvement of 10Hz).

Note that capacitor and resistor values used in the simulation of the amplifier were set exactly to the calculated value and not available practical values (e.g. C_1 is 311.21μF, but in the real world 330μF would have to be used). The reason why practical values were not used is because a more complete comparison could be made.

It is clear that simulation programs like PSpice are extremely useful as they can be used to test and improve amplifier circuit designs easily and cheaply. It is also clear that the ROT (Rules of Thumb) used in the design of this amplifier work well, which resulted in a reasonable good amplifier design. As computers get more and more powerful, simulators will become more powerful making the life of the design engineer easier and perhaps in-time these programs will be able to design circuits automatically from some technical specifications.

APPENDIX 1 – PSPICE OUTPUT FILE

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**** 11/11/01 13:13:03 *********** Evaluation PSpice (Nov 1999) **************

 * C:\Work\Colin\EDUCATIONAL WORK\Beng (hons) electronics systems\Year
4\Assigment\Electronic Circuit Design\Analog\Ass1\pSpice\Cricu


 ****     CIRCUIT DESCRIPTION


******************************************************************************




* Schematics Version 9.1 - Web Update 1
* Sat Nov 10 20:59:01 2001



** Analysis setup **
.ac DEC 1000 1 10MEG
.OP
.STMLIB "Schematic1.stl"


* From [PSPICE NETLIST] section of pspiceev.ini:
.lib "nom.lib"

.INC "Cricuit1.net"

**** INCLUDING Cricuit1.net ****
* Schematics Netlist *



R_RL         0 $N_0001  1k
R_R         $N_0003 $N_0002  10k
R_RC         $N_0005 $N_0004  5k
R_R1         $N_0006 $N_0004  1MEG
R_R2         0 $N_0006  500k
J_J1         $N_0004 $N_0006 $N_0007 J2N3819
Q_Q1         $N_0005 $N_0007 $N_0008 Q2N2222
V_V2         $N_0004 0 15V
V_V         $N_0003 0 DC 0V AC 500mV
R_RS         0 $N_0007  2.6k
R_RE         0 $N_0008  5.8k
C_CE         0 $N_0008  311.21u
C_C1         $N_0002 $N_0006  24.2n
C_C2         $N_0001 $N_0005  1.46u

**** RESUMING Cricuit1.cir ****
.INC "Cricuit1.als"



**** INCLUDING Cricuit1.als ****
* Schematics Aliases *

.ALIASES
R_RL            RL(1=0 2=$N_0001 )
R_R             R(1=$N_0003 2=$N_0002 )
R_RC            RC(1=$N_0005 2=$N_0004 )
R_R1            R1(1=$N_0006 2=$N_0004 )
R_R2            R2(1=0 2=$N_0006 )
```

```
J_J1            J1(d=$N_0004 g=$N_0006 s=$N_0007 )
Q_Q1            Q1(c=$N_0005 b=$N_0007 e=$N_0008 )
V_V2            V2(+=$N_0004 -=0 )
V_V             V(+=$N_0003 -=0 )
R_RS            RS(1=0 2=$N_0007 )
R_RE            RE(1=0 2=$N_0008 )
C_CE            CE(1=0 2=$N_0008 )
C_C1            C1(1=$N_0002 2=$N_0006 )
C_C2            C2(1=$N_0001 2=$N_0005 )
.ENDALIASES


**** RESUMING Cricuit1.cir ****
.probe


.END

**** 11/11/01 13:13:03 *********** Evaluation PSpice (Nov 1999) **************

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4\Assigment\Electronic Circuit Design\Analog\Ass1\pSpice\Cricu


 ****     BJT MODEL PARAMETERS


******************************************************************************




               Q2N2222
               NPN
          IS   14.340000E-15
          BF  255.9
          NF    1
         VAF   74.03
         IKF     .2847
         ISE   14.340000E-15
          NE    1.307
          BR    6.092
          NR    1
          RB   10
          RC    1
         CJE   22.010000E-12
         MJE     .377
         CJC    7.306000E-12
         MJC     .3416
          TF  411.100000E-12
         XTF    3
         VTF    1.7
         ITF     .6
          TR   46.910000E-09
         XTB    1.5
          CN    2.42
           D     .87

**** 11/11/01 13:13:03 *********** Evaluation PSpice (Nov 1999) **************

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 ****     Junction FET MODEL PARAMETERS

******************************************************************************



               J2N3819
               NJF
         VTO   -3
        BETA    1.304000E-03
      LAMBDA    2.250000E-03
          IS   33.570000E-15
         ISR  322.400000E-15
       ALPHA  311.700000E-06
          VK  243.6
          RD    1
          RS    1
         CGD    1.600000E-12
         CGS    2.414000E-12
           M     .3622
       VTOTC   -2.500000E-03
     BETATCE    -.5
          KF    9.882000E-18

**** 11/11/01 13:13:03 *********** Evaluation PSpice (Nov 1999) **************

 * C:\Work\Colin\EDUCATIONAL WORK\Beng (hons) electronics systems\Year
4\Assigment\Electronic Circuit Design\Analog\Ass1\pSpice\Cricu


 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

******************************************************************************



 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE


($N_0001)    0.0000                   ($N_0002)    0.0000

($N_0003)    0.0000                   ($N_0004)   15.0000

($N_0005)    9.8894                   ($N_0006)    5.0000

($N_0007)    6.6121                   ($N_0008)    5.9667




    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V2        -3.582E-03
    V_V          0.000E+00

    TOTAL POWER DISSIPATION   5.37E-02  WATTS

**** 11/11/01 13:13:03 *********** Evaluation PSpice (Nov 1999) **************

 * C:\Work\Colin\EDUCATIONAL WORK\Beng (hons) electronics systems\Year
4\Assigment\Electronic Circuit Design\Analog\Ass1\pSpice\Cricu
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```
 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

******************************************************************************




**** BIPOLAR JUNCTION TRANSISTORS


NAME         Q_Q1
MODEL        Q2N2222
IB            6.64E-06
IC            1.02E-03
VBE           6.45E-01
VBC          -3.28E+00
VCE           3.92E+00
BETADC        1.54E+02
GM            3.94E-02
RPI           4.33E+03
RX            1.00E+01
RO            7.56E+04
CBE           5.25E-11
CBC           4.11E-12
CJS           0.00E+00
BETAAC        1.70E+02
CBX/CBX2      0.00E+00
FT/FT2        1.11E+08



**** JFETS


NAME         J_J1
MODEL        J2N3819
ID            2.55E-03
VGS          -1.61E+00
VDS           8.39E+00
GM            3.68E-03
GDS           5.63E-06
CGS           1.70E-12
CGD           6.71E-13

          JOB CONCLUDED

          TOTAL JOB TIME            1.39
```

N-Channel JFET

PRODUCT SUMMARY			
$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (MS)	I_{DSS} MIN (MA)
≤ –8	–25	2	2

FEATURES

- Excellent High-Frequency Gain: Gps 11 dB @ 400 MHz
- Very Low Noise: 3 dB @ 400 MHz
- Very Low Distortion
- High ac/dc Switch Off-Isolation
- High Gain: A_V = 60 @ 100 μA

BENEFITS

- Wideband High Gain
- Very High System Sensitivity
- High Quality of Amplification
- High-Speed Switching Capability
- High Low-Level Signal Amplification

APPLICATIONS

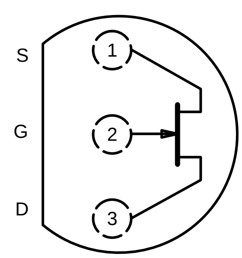
- High-Frequency Amplifier/Mixer
- Oscillator
- Sample-and-Hold
- Very Low Capacitance Switches

DESCRIPTION

The 2N3819 is a low-cost, all-purpose JFET which offers good performance at mid-to-high frequencies. It features low noise and leakage and guarantees high gain at 100 MHz.

Its TO-226AA (TO-92) package is compatible with various tape-and-reel options for automated assembly (see Packaging Information). For similar products in TO-206AF (TO-72) and TO-236 (SOT-23) packages, see the 2N4416/2N4416A/SST4416 data sheet.

TO-226AA
(TO-92)



Top View

ABSOLUTE MAXIMUM RATINGS

Gate-Source/Gate-Drain Voltage . . . . –25 V
Forward Gate Current . . . . 10 mA
Storage Temperature . . . . –55 to 150°C
Operating Junction Temperature . . . . –55 to 150°C

Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . 300°C
Power Dissipation[A] . . . . 350 mW

Notes
A. Derate 2.8 mW/°C above 25°C

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70238.

SPECIFICATIONS[A]

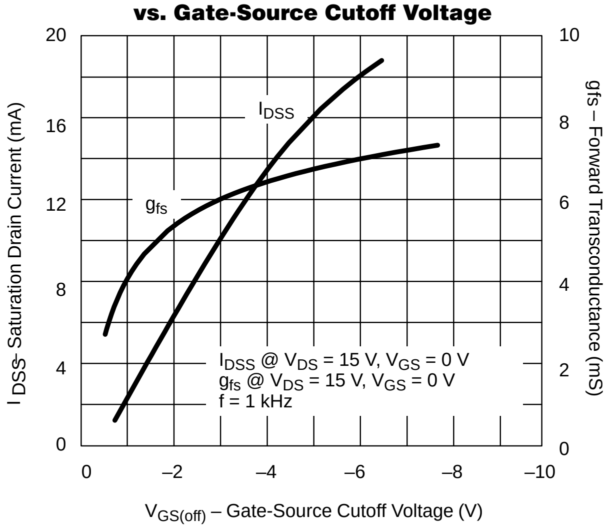
PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP[B]	LIMITS MAX	UNIT
STATIC							
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 μA , V_{DS} = 0 V		–25	–35		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 2 nA			–3	–8	V
Saturation Drain Current[C]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		2	10	20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = –15 V, V_{DS} = 0 V			–0.002	–2	nA
			T_A = 100°C		–0.002	–2	μA
Gate Operating Current[D]	I_G	V_{DG} = 10 V, I_D = 1 mA			–20		pA
Drain Cutoff Current	$I_{D(off)}$	V_{DS} = 10 V, V_{GS} = –8 V			2		pA
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, I_D = 1 mA			150		Ω
Gate-Source Voltage	V_{GS}	V_{DS} = 15 V, I_D = 200 μA		–0.5	–2.5	–7.5	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V			0.7		V
DYNAMIC							
Common-Source Forward Transconductance[D]	g_{fs}	V_{DS} = 15 V V_{GS} = 0 V	f = 1 kHz	2	5.5	6.5	mS
			f = 100 MHz	1.6	5.5		mS
Common-Source Output Conductance[D]	g_{os}	V_{DS} = 15 V V_{GS} = 0 V	f = 1 kHz		25	50	μS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz			2.2	8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz			0.7	4	pF
Equivalent Input Noise Voltage[D]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz			6		$nV/\sqrt{Hz}$

Notes
A. T_A = 25°C unless otherwise noted.
B. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
C. Pulse test: PW ≤300 μs, duty cycle ≤2%.
D. This parameter not registered with JEDEC.

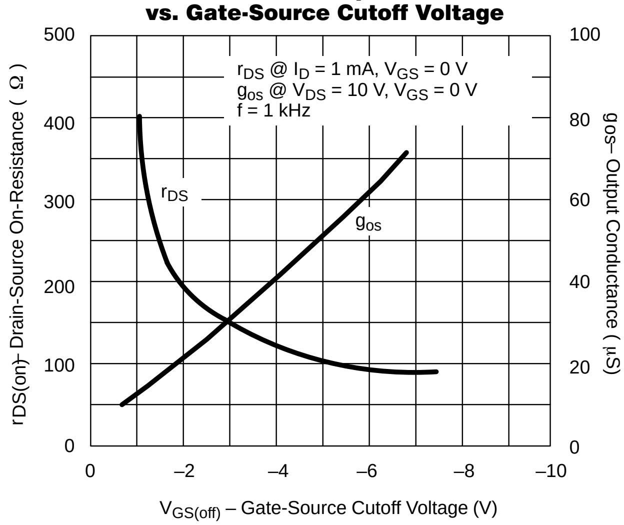
NH

TYPICAL CHARACTERISTICS

Drain Current and Transconductance vs. Gate-Source Cutoff Voltage

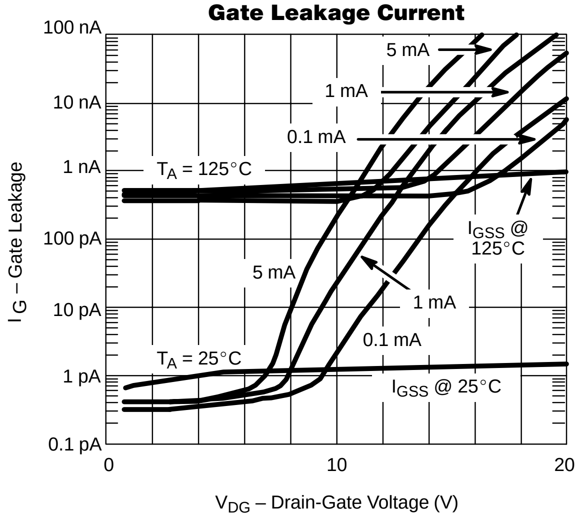


On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage

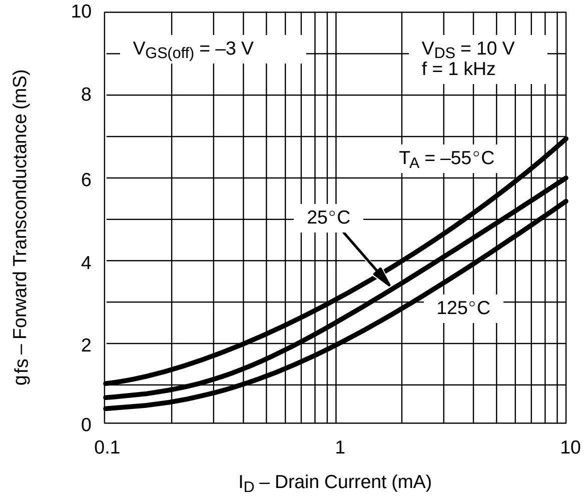


TYPICAL CHARACTERISTICS

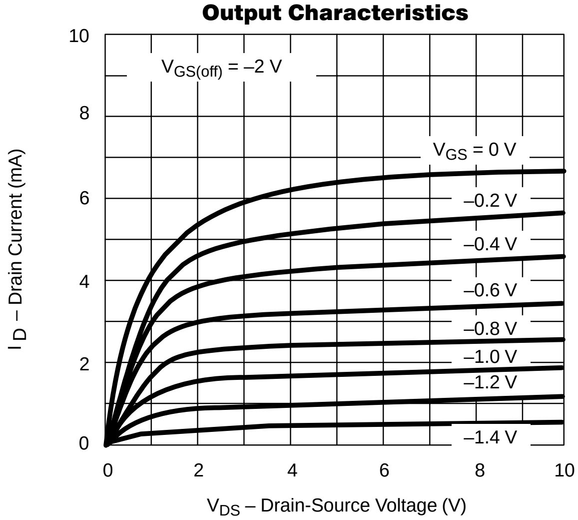
Gate Leakage Current



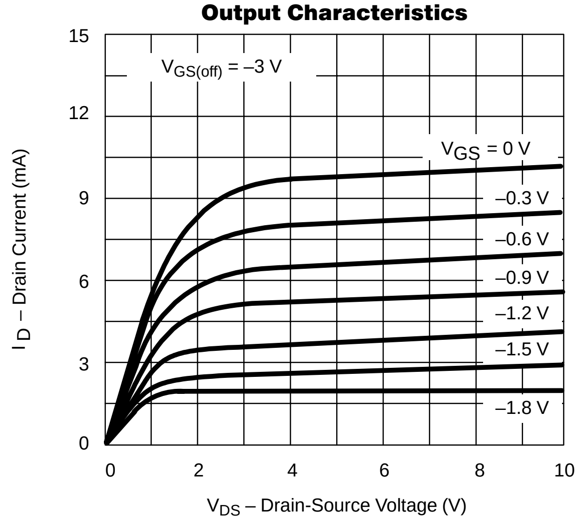
Common-Source Forward Transconductance vs. Drain Current



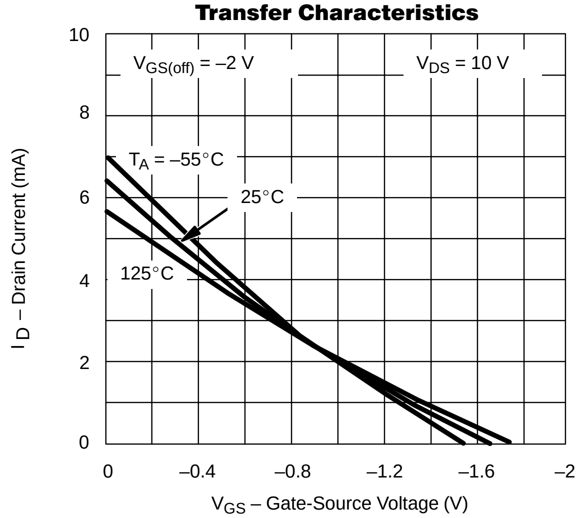
Output Characteristics



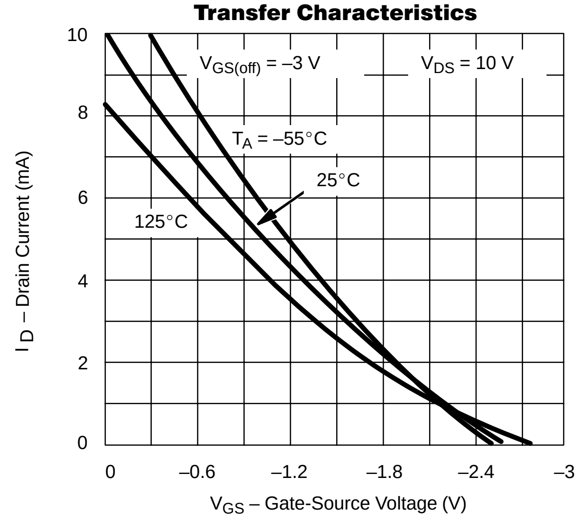
Output Characteristics



Transfer Characteristics

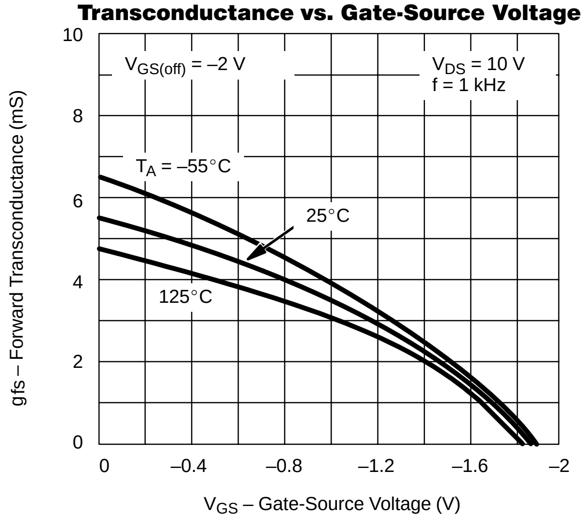


Transfer Characteristics

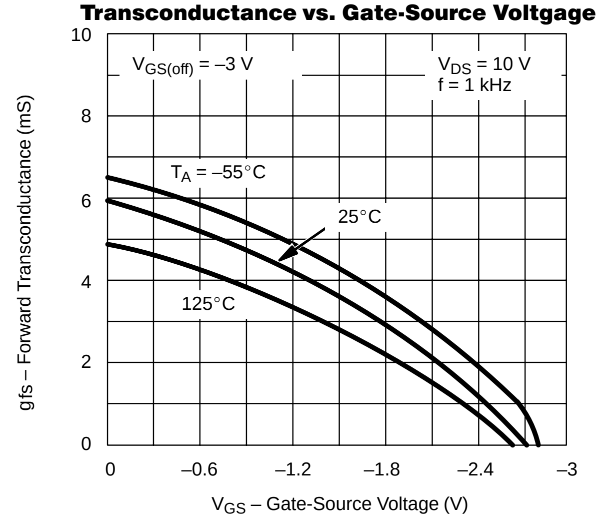


TYPICAL CHARACTERISTICS

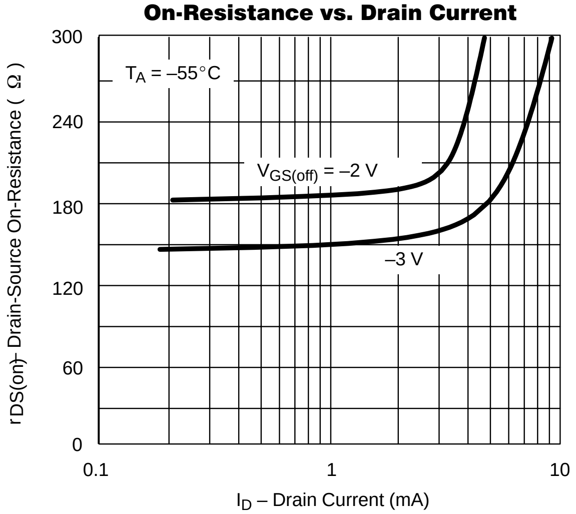
Transconductance vs. Gate-Source Voltage



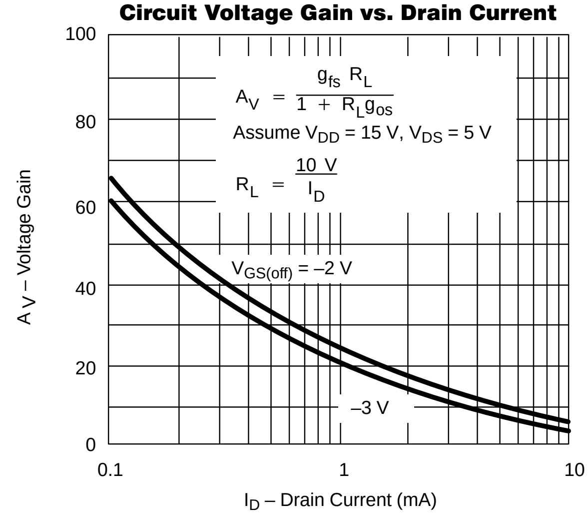
Transconductance vs. Gate-Source Voltgage



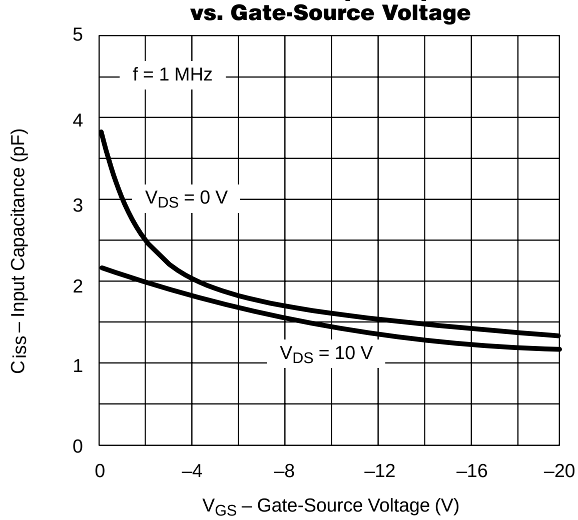
On-Resistance vs. Drain Current



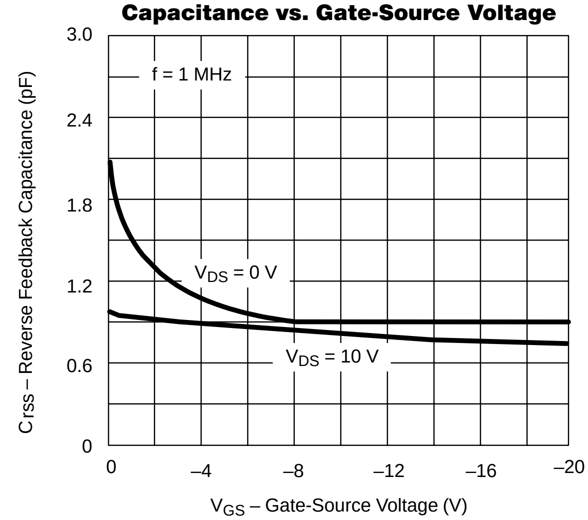
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage

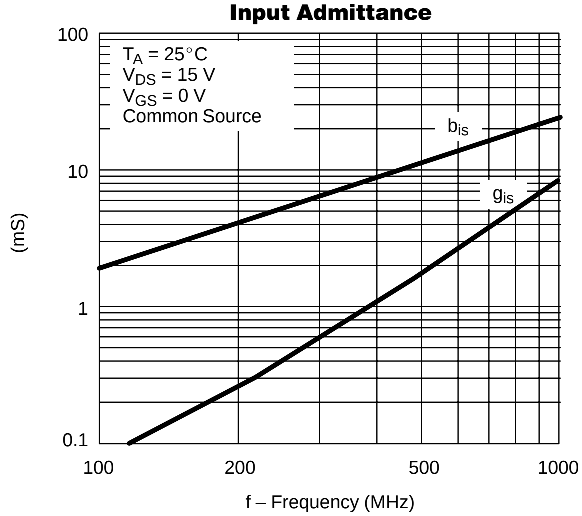


Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage

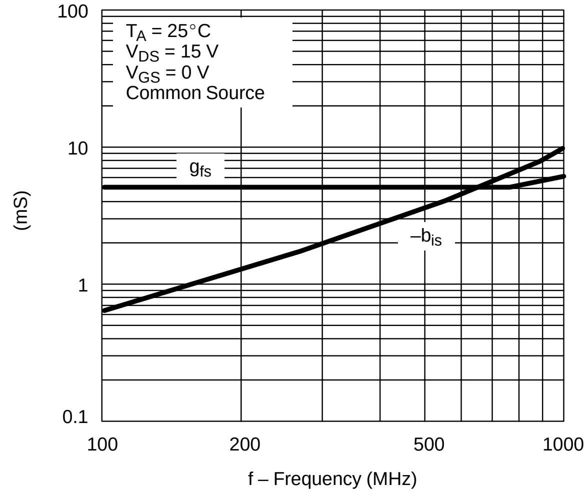


TYPICAL CHARACTERISTICS

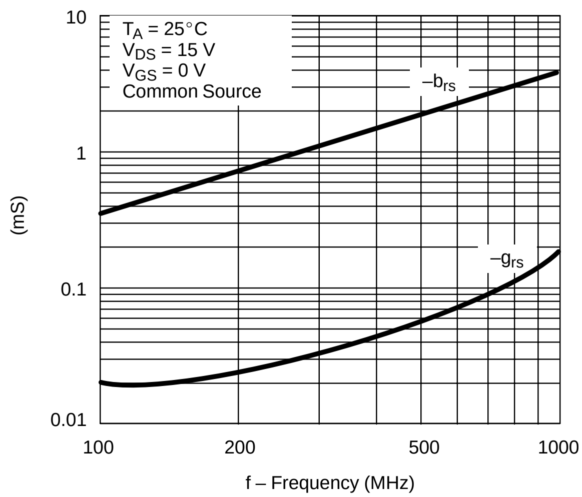
Input Admittance



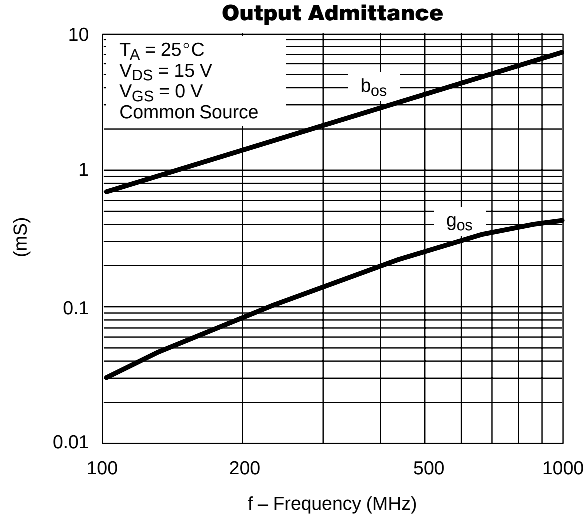
Forward Admittance



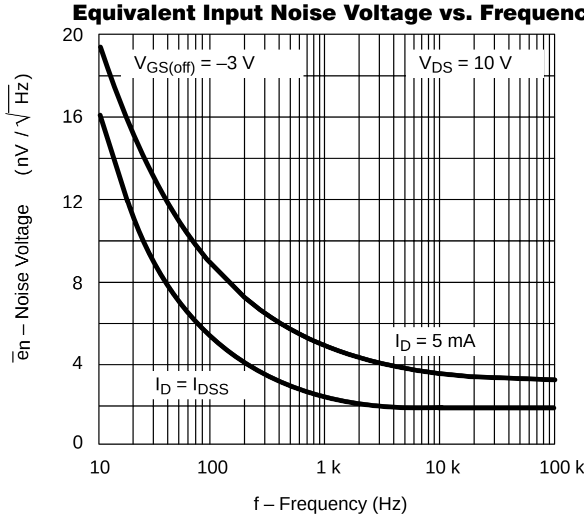
Reverse Admittance



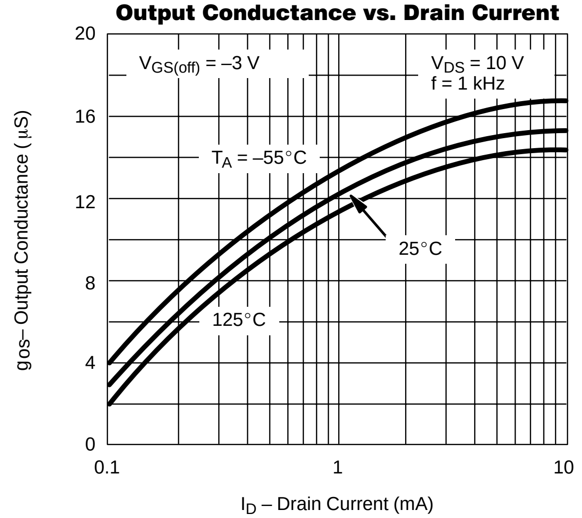
Output Admittance



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



SGS-THOMSON MICROELECTRONICS

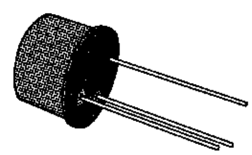
2N2218-2N2219
2N2221-2N2222

HIGH-SPEED SWITCHES

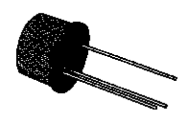
DESCRIPTION

The 2N2218, 2N2219, 2N2221 and 2N2222 are silicon planar epitaxial NPN transistors in Jedec TO-39 (for 2N2218 and 2N2219) and in Jedec TO-18 (for 2N2221 and 2N2222) metal cases. They are designed for high-speed switching applications at collector currents up to 500 mA, and feature useful current gain over a wide range of collector current, low leakage currents and low saturation voltages.

2N2218/2N2219 approved to CECC 50002-100, 2N2221/2N2222 approved to CECC 50002-101 available on request.

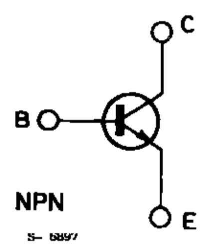


TO-39



TO-18

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base Voltage (I_E = 0)	60	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	30	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5	V
I_C	Collector Current	0.8	A
P_{tot}	Total Power Dissipation at $T_{amb} \leq 25$ °C		
	for **2N2218** and **2N2219**	0.8	W
	for **2N2221** and **2N2222**	0.5	W
	at $T_{case} \leq 25$ °C		
	for **2N2218** and **2N2219**	3	W
	for **2N2221** and **2N2222**	1.8	W
T_{stg}	Storage Temperature	– 65 to 200	°C
T_j	Junction Temperature	175	°C

THERMAL DATA

			2N2218 2N2219	2N2221 2N2222
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	50 °C/W	83.3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	187.5 °C/W	300 °C/W

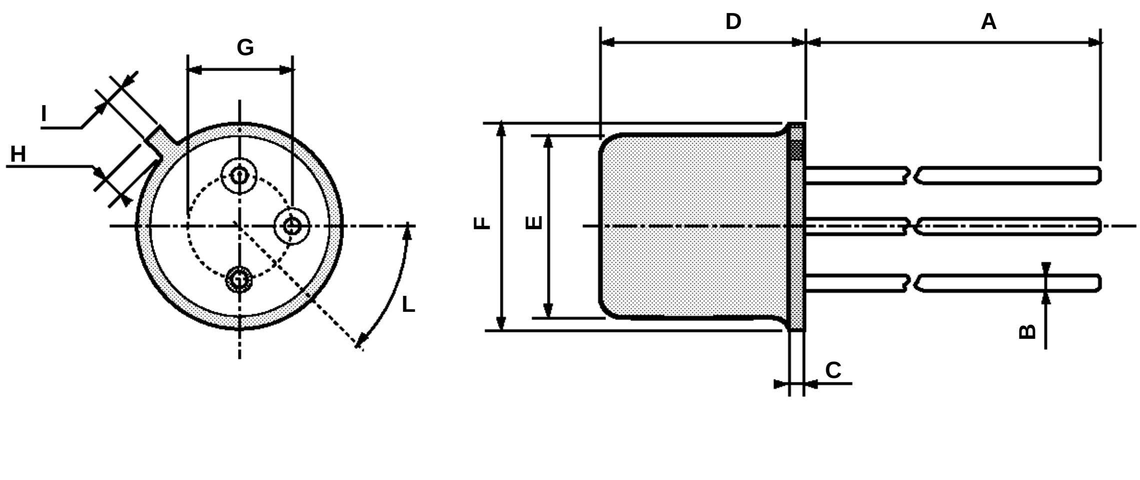
ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cutoff Current (I_E = 0)	V_{CB} = 50 V V_{CB} = 50 V T_{amb} = 150 °C			10 10	nA μA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 3 V			10	nA
$V_{(BR)\ CBO}$	Colllector-base Breakdown Voltage (I_E = 0)	I_C = 10 μA	60			V
$V_{(BR)CEO}$*	Collector-emitter Breakdown Voltage (I_B = 0)	I_C = 10 mA	30			V
$V_{(BR)\ EBO}$	Emittter-base Breakdown Voltage (I_C = 0)	I_E = 10 μA	5			V
$V_{CE\ (sat)}$*	Collector-emitter Saturation Voltage	I_C = 150 mA I_B = 15 mA I_C = 500 mA I_B = 50 mA			0.4 1.6	V V
$V_{BE\ (sat)}$*	Base-emitter Saturation Voltage	I_C = 150 mA I_B = 15 mA I_C = 500 mA I_B = 50 mA			1.3 2.6	V V
h_{FE}*	DC Current Gain	for **2N2218** and **2N2221** I_C = 0.1 mA V_{CE} = 10 V I_C = 1 mA V_{CE} = 10 V I_C = 10 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 10 V I_C = 500 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 1 V for **2N2219** and **2N2222** I_C = 0.1 mA V_{CE} = 10 V I_C = 1 mA V_{CE} = 10 V I_C = 10 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 10 V I_C = 500 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 1 V	 20 25 35 40 20 20 35 50 75 100 30 50		 120 300	
f_T	Transition Frequency	I_C = 20 mA V_{CE} = 20 V f = 100 MHz	250			MHz
C_{CBO}	Collector-base Capacitance	I_E = 0 V_{CB} = 10 V f = 100 kHz			8	pF
$R_{e(hie)}$	Real Part of Input Impedance	I_C = 20 mA V_{CE} = 20 V f = 300 MHz			60	Ω

* Pulsed : pulse duration = 300 μs, duty cyde = 1 %.

TO-18 MECHANICAL DATA

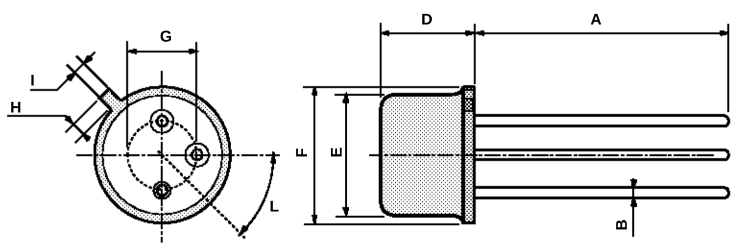
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		12.7			0.500	
B			0.49			0.019
D			5.3			0.208
E			4.9			0.193
F			5.8			0.228
G	2.54			0.100		
H			1.2			0.047
I			1.16			0.045
L	45^o			45^o		



0016043

TO39 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.7			0.500		
B			0.49			0.019
D			6.6			0.260
E			8.5			0.334
F			9.4			0.370
G	5.08			0.200		
H			1.2			0.047
I			0.9			0.035
L	45^o (typ.)					



P008B

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